Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Cancelled)

6. (Previously Presented) A method for fabricating an integrated circuit, comprising the steps of:

forming a plurality of CMOS polysilicon gate structures over a semiconductor body;

forming a gate dielectric on said semiconductor body prior to forming the plurality of CMOS polysilicon gate structures such that said gate dielectric is located between said semiconductor body and said plurality of CMOS polysilicon gate structures;

forming a layer of nickel over said semiconductor body including over said plurality of CMOS polysilicon gate structures;

forming a capping layer over said layer of nickel, said capping layer comprising a material with an affinity for boron;

then, annealing the semiconductor body to completely convert said CMOS polysilicon gate structures into NiSi gate electrodes; and

removing said capping layer and unreacted portions of said layer of nickel, wherein said capping layer attracts a significant amount of boron away from an interface with said gate dielectric in a PMOS transistor but does not attract a significant amount of arsenic away from an interface with said gate dielectric in an NMOS transistor during said annealing step.

7-8. (Cancelled)

9. (Original) A method for fabricating an integrated circuit, comprising the steps of:

providing a semiconductor body having a plurality of polysilicon gate structures formed there on, wherein a first subset of said plurality of polysilicon gate structures are doped with boron dopant and a second subset of said plurality of polysilicon gate structures are doped with arsenic dopant;

forming a nickel layer over said semiconductor body including over said plurality of polysilicon gate structures;

forming a capping layer over said nickel layer, said capping layer comprising a transition metal nitride with an affinity for boron;

then, annealing the semiconductor body to completely convert said polysilicon gate structures to NiSi gate electrodes by reacting portions of said nickel layer with said polysilicon gate structures, wherein boron is redistributed during the annealing step with portion of the boron diffusing into said capping layer; and

removing said capping layer and unreacted portions of said layer of nickel.

10. (Original) The method of claim 9, wherein said transition metal-nitride comprises TiN.

11. (Original) The method of claim 10, wherein said annealing step is performed at a temperature in the range of 400°C to 600°C.